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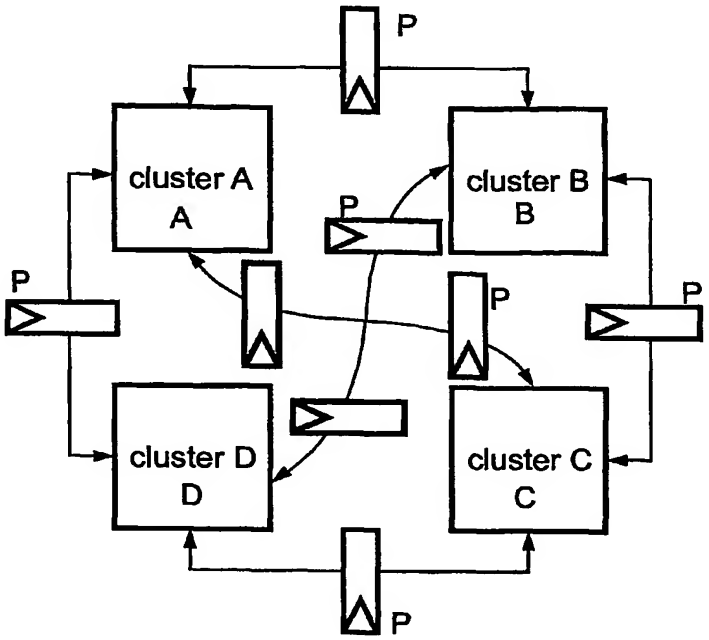
(54) Title: CLUSTERED ILP PROCESSOR



(57) Abstract: The basic idea of the invention is to provide a clustered ILP processor based on a fully-connected inter-cluster network with a non-uniform latency. A clustered Instruction Level Parallelism processor is provided. Said processor comprises a plurality of clusters (C1 - C6) each comprising at least one register file (RF) and at least one functional unit (FU), wherein said clusters (C1 - C6) are fully-connected to each other; and wherein the latency of the connections between said clusters (C1 - C6) depends on the distance between said clusters (C1 - C6).

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